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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/023,235	12/17/2001	Kerry Bernstein	BUR9-2001-0178-US1	3714
29154 FREDERICK	29154 7590 09/12/2007 FREDERICK W. GIBB, III		EXAMINER	
Gibb & Rahman, LLC			SAXENA, AKASH	
2568-A RIVA ROAD SUITE 304		ı	ART UNIT	PAPER NUMBER
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Application No. Applicant(s) **Advisory Action** 10/023,235 BERNSTEIN ET AL. Before the Filing of an Appeal Brief Examiner **Art Unit** Akash Saxena 2128 --The MAILING DATE of this communication appears on the cover sheet with the correspondence address --THE REPLY FILED 28 August 2007 FAILS TO PLACE THIS APPLICATION IN CONDITION FOR ALLOWANCE. 1. X The reply was filed after a final rejection, but prior to or on the same day as filing a Notice of Appeal. To avoid abandonment of this application, applicant must timely file one of the following replies: (1) an amendment, affidavit, or other evidence, which places the application in condition for allowance; (2) a Notice of Appeal (with appeal fee) in compliance with 37 CFR 41.31; or (3) a Request for Continued Examination (RCE) in compliance with 37 CFR 1.114. The reply must be filed within one of the following time periods: a) The period for reply expires months from the mailing date of the final rejection. b) 💢 The period for reply expires on: (1) the mailing date of this Advisory Action, or (2) the date set forth in the final rejection, whichever is later. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of the final rejection. Examiner Note: If box 1 is checked, check either box (a) or (b). ONLY CHECK BOX (b) WHEN THE FIRST REPLY WAS FILED WITHIN TWO MONTHS OF THE FINAL REJECTION. See MPEP 706.07(f). Extensions of time may be obtained under 37 CFR 1.136(a). The date on which the petition under 37 CFR 1.136(a) and the appropriate extension fee have been filed is the date for purposes of determining the period of extension and the corresponding amount of the fee. The appropriate extension fee under 37 CFR 1.17(a) is calculated from: (1) the expiration date of the shortened statutory period for reply originally set in the final Office action; or (2) as set forth in (b) above, if checked. Any reply received by the Office later than three months after the mailing date of the final rejection, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b). NOTICE OF APPEAL 2. The Notice of Appeal was filed on _____. A brief in compliance with 37 CFR 41.37 must be filed within two months of the date of filing the Notice of Appeal (37 CFR 41.37(a)), or any extension thereof (37 CFR 41.37(e)), to avoid dismissal of the appeal. Since a Notice of Appeal has been filed, any reply must be filed within the time period set forth in 37 CFR 41.37(a). **AMENDMENTS** 3. The proposed amendment(s) filed after a final rejection, but prior to the date of filing a brief, will not be entered because (a) They raise new issues that would require further consideration and/or search (see NOTE below): (b) They raise the issue of new matter (see NOTE below): (c) They are not deemed to place the application in better form for appeal by materially reducing or simplifying the issues for appeal; and/or (d) They present additional claims without canceling a corresponding number of finally rejected claims. NOTE: . (See 37 CFR 1.116 and 41.33(a)). 4. The amendments are not in compliance with 37 CFR 1.121. See attached Notice of Non-Compliant Amendment (PTOL-324). 5. Applicant's reply has overcome the following rejection(s): 6. Newly proposed or amended claim(s) _____ would be allowable if submitted in a separate, timely filed amendment canceling the non-allowable claim(s). 7 × For purposes of appeal, the proposed amendment(s): a) × will not be entered, or b) will be entered and an explanation of how the new or amended claims would be rejected is provided below or appended. The status of the claim(s) is (or will be) as follows: Claim(s) allowed: Claim(s) objected to: Claim(s) rejected: 1-3,5-11,13-22 and 24-42. Claim(s) withdrawn from consideration: _____. AFFIDAVIT OR OTHER EVIDENCE 8. The affidavit or other evidence filed after a final action, but before or on the date of filing a Notice of Appeal will not be entered

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13. Other:

was not earlier presented. See 37 CFR 1.116(e).

REQUEST FOR RECONSIDERATION/OTHER

See Continuation Sheet.

because applicant failed to provide a showing of good and sufficient reasons why the affidavit or other evidence is necessary and

entered because the affidavit or other evidence failed to overcome all rejections under appeal and/or appellant fails to provide a

9. The affidavit or other evidence filed after the date of filing a Notice of Appeal, but prior to the date of filing a brief, will not be

11. X The request for reconsideration has been considered but does NOT place the application in condition for allowance because:

showing a good and sufficient reasons why it is necessary and was not earlier presented. See 37 CFR 41.33(d)(1).

10. The affidavit or other evidence is entered. An explanation of the status of the claims after entry is below or attached.

12. Note the attached Information Disclosure Statement(s). (PTO/SB/08) Paper No(s).

Continuation of 11. does NOT place the application in condition for allowance because:

Applicant has argued rejection made under 35 USC 112 first paragraph to be enabled by specification [0023], [0025, [0026], [0034], [0035] and [0038]. Examiner respectfully disagrees that aforementioned paragraphs actually teach how the target model is created using performance parameter ranges. Further applicant's have pointed out claims 14, 19 and 36 are not limited to "a computer model" therefore the rejection under this statute is not warrented. Examiner disagrees with applicant as claims 14, 19 and 36 all disclose "producing a target model" (claim 14), "target model is created" (Claim 19) and "tangibly embodying a model of an integrated circuit device" (claim 36), none of which have support in the specification and are correctly rejected under this statute.

Applicant has argued against rejections made under 35 USC 112 second paragraph, stating "While no specific ranges are provided in the claims, none are required. The ranges are application specific.". Examiner while can appreciate the difficulty in claiming such ranges (ranges in manufacturing process variations) which is application or process specific, however such limitations are extremely difficult to interpret unless claimed more specifically. Support in the specification [0020]-[0030] and associated ifigures is noted, however none of which are specifically claimed or referred to in the claim. The figures are also not specific in the values which these ranges bound. Examiner maintains the rejection.

Applicant has argued against the rejection made under 35 USC 103 that Hershenson does not teach or disclose that a target model for the device is created using a target performance parameter range for a given performance attribute of that device. Examiner disagrees as First, Hershenson teaches bounded range for the process variations (Hershenson Col.3 Line 67-Col.4 Line 39; Col.7 Lines 30-50; Col.21 Lines 44-58). As for process variations based on a corresponding one of the multiple model curves for different designs of said device, Hershenson teaches various circuit topologies performing the same function but optimized for various performance points (Hershenson: at least Col.5 Lines 40 -Col.6 Lines 24).

KR'527 teaches a semiconductor process simulator (KR'527: Fig.6a Element 620) and process parameters for individual processes (KR'527: Fig.6a Elements 602a-e) are sampled in and or simulated from the Monte Carlo Engine (KR'527: Fig.6b Elements 690, 693-695, 620). Range bounds are also provided (Abstract: Lines 19-27; Col.8 Lines 50-63). Arguements related to the a target model for the device is created using a target performance parameter range for a given performance attribute of that device are taught by Hershenson above.

On pages 27-28 of the remarks applicants have argued the following: "Additionally, the referred to values of parameters (e.g., transistor threshold voltages, mobilities, oxide parameters, channel modulations parameters, supply voltages, and load capacitances) correspond to specifications for a circuit and not to the specifications for a device (e.g., a transistor) that is incorporated into the circuit, as in the present invention." Examiner finds the arguement unpersuasive as by applicant own example transistor threshold voltage is not parameter of device (e.g. transistor).

Further applicant disagrees that Hershenson teaches or suggests that target model for the device within the integrated circuit is created using target performance parameter range for a performance atttribute of the device, but merely selects the device and then the geometric program is generated. Examiner is unclear what is entailed in the generation of the target model (See 112¶1st above) therefore the generation of the geometric model at present is best understood as the creation of the target model for the device within the integrated circuit.

Applicant has further stated that on Pg.30 of remarks that the second bounded range in Hershenson Col.6 Lines 1-24 is not shown. Examiner disagrees, specifically, Hershenson teaches the second bounded range due to various device topologies (Col.6 Lines 22-24; Col.5 Lines 40-48).

Examiner has briefly addressed applicants remarks above and disagrees with the applicants for at least the reasons presented above.

Akash Saxena 9/5/07

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